Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination – June – 2017**

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| **Code :** | **14EC3054** | **Duration :** | **3hrs** |
| **Sub. Name :** | **HARDWARE DESIGN VERIFICATION TECHNIQUES** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Construct a source code and illustrate the need of linting tool for hardware verification. | CO2 | 14 |
| b. | Predict the metrics that are related with the functional verification that other productivity metrics. | CO2 | 6 |
| (OR) | | | | |
| 2. | a. | Describe in detail about third party models. | CO1 | 6 |
| b. | Discuss in detail about the necessary of simulators. | CO1 | 6 |
| c. | Some designs have very few inputs and output, but have a large number of possible states, requiring long sequences to properly observe and control all internal physical locations .Choose a suitable testing method and discuss the same. | CO1 | 8 |
| 3. | a. | Identify the coverage that measures all possible ways to execute the sequence of statements. | CO1 | 8 |
|  | b. | Describe in detail about Co-Simulators. | CO2 | 6 |
|  | c. | Identify the system, in which issues are formally reported, usually through free-form documents such as e-mail messages | CO1 | 6 |
| (OR) | | | | |
| 4. | a. | With neat diagram distinguish in detail about levels of verification. | CO1 | 8 |
|  | b. | Suggest about first-time success, how a design is verified, and which test benches are written-Discuss in detail about the verification plan. | CO2 | 12 |
| 5. | a. | Discuss in detail about Verification strategies. | CO1 | 8 |
|  | b. | Recognize in detail about Random Verification. | CO1 | 6 |
|  | c. | The primary objective of a particular verification is to confirm that the connectivity captured by the board design tool is correct. With neat diagram discuss about the verification. | CO3 | 6 |
| (OR) | | | | |
| 6. | a. | All design teams have informal systems to track issues and ensure their resolutions. Find the issues and check the functionality of the design. | CO2 | 14 |
|  | b. | The application of synchronous data can be encapsulated. With neat waveform and source code deliberate in detail about the condition described above. | CO2 | 6 |
| 7. | a. | Predict how a zero delay and Non-zero delay waveforms are generated in Synchronous circuits? | CO1 | 8 |
|  | b. | Describe in detail about design for Verification. | CO3 | 12 |
| (OR) | | | | |
| 8. | a. | Analyze in detail about self checking test benches. | CO2 | 6 |
|  | b. | How will you decide applying the stimulus is relatively easy and how will you plan to determine the expected response. Describe in detail. | CO2 | 8 |
|  | c. | Discuss about the errors to consider when verifying from specification to features. | CO2 | 6 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Ilustrate in detail about Combining eVCs and give its uses. | CO3 | 12 |
|  | b. | Describe briefly Reusable Verification Components(eVCs),Clocks ,Events,DUT Signals and Agent Details. | CO3 | 8 |

**ALL THE BEST**